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REMARKS

In this Office Action, Claims 1-30 are pending and stand rejected. Claim 27, FIGS 1 and 9 are objected to by the Examiner. In response, Applicants amend the Specification, FIG 1 and 9. Claims 1, 11, 21, 26 and 27 are amended, no claims are added, and no claims are cancelled. Accordingly, claims 1-30 are pending. Applicants respectfully request reconsideration in view of the following remarks and the above amendments

I. Objections to Drawings

The Examiner objected to FIG. 1 for failing to comply with 37 CFR 1.84(p)(4) because reference character "160" has been used to designate both ICH and HDD. In addition, the Examiner also objected to drawings for failing to comply with 37 CFR 1.84(p)(5) because the following reference characters not mentioned in the description: 102, 132, 142 in FIG. 1 and 442 in FIG. 9.

Applicants amend Specification and FIGS 1 to include the reference characters 104 and 106 and to refer to reference characters, 132, 142 and 442 and respectfully request that the Examiner withdraw objections to drawings.

II. Claim Objections

Claim 27 is objected to for the following informalities: A comma is present where a period where a period should be. Applicants amend Claim 27 to correct the informality and respectfully request withdrawal objection to Claim 27.

III. Claims Rejected Under 35 U.S.C. § 102(e)

Claims 1-30 are rejected under35 U.S.C. § 102(e) as being allegedly anticipated over U.S. Patent No. 6,807,616 issued to McGrath (hereinafter "McGrath"). Applicants respectfully traverse this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim features which are neither expressly nor inherently disclosed by McGrath:

translating instructions from a source instruction set architecture (ISA) having a segmented memory addressing model into a target ISA of a target architecture having only a non-segmented memory addressing model;

assigning, during the translation of the instructions, at least one target architecture predicate register to identify a target architecture register containing a base address of a segment associated with a logical address of a translated instruction;

executing the translated instructions; and

simulating, during execution of the translated instruction, a segmented addressing model within the target architecture for the translated instructions to enable conversion of the logical addresses of the translated instructions to effective addresses of the target architecture. (Emphasis added.)

McGrath is generally directed to memory address checking in a processor that is support both a segmented and un-segmented address apace. In contrast with Claim 1, McGrath does not teach or suggest a target architecture that supports only a non-segmented memory addressing model, much less a translator that assigns a target architecture predicate register to identify a target architecture register containing a base address of a segment associated with a logical address of a translated instruction, as in Claim 1.

In one embodiment, McGrath discloses a memory management unit (MMU) 20 which provides architectural features such as segment registers 24, a local distributor table register (LDTR) 30 and a global descriptor table register (GDTR) 32 to provide architectural resources for supporting a segmented memory addressing model. Hence, in accordance with such embodiment, the target architecture taught by McGrath supports a segmented address space in contrast with Claim 1, which recites a target architecture having only a non-segmented memory addressing model.

Although McGrath describes embodiments which do not provide architectural support for implementing a segmented address space, such as the embodiment shown in FIGS 12-13. As shown in FIGS. 12 and 14, all of the non-native architecture state is mapped to memory including descriptive tables 1046, page tables 1048, task state segments 1050, general registers 1052, segment registers 1054, control registers 1056 and other registers 1058 to represent the non-native architecture state. (See col. 3, lines 31-39.)

Applicants respectfully submit that memory mapping illustrated with reference to FIGS. 12 and 13 fails to teach or suggest the assignment of a target architecture predicate register to

identify a target register containing a base address of a segment associated with a logical address of a translated instruction, as in Claim 1. We submit that such register assignment as in Claim 1 provides improved efficiency for the translation of logical addresses to their effective addresses for operation according to the non-segmented addressing model of the target architecture, as in Claim 1. Conversely, the embodiments illustrated with reference to FIGS. 12 and 13 of McGrath require access to memory to provide such effective address calculation which may be inefficient in comparison to the register assignment recited by amended Claim 1.

In the embodiment of McGrath disclosed in FIG. 14, the processor 1042 includes at least segment registers which are implemented in hardware of the processor. As disclosed by McGrath, processor 1042 may not only implements storage for segment registers 1054, but may also include logic to generate the operating mode for instructions based on the information of the segment registers. (See col. 24, lines 26-39.) Apposite to Claim 1, segment registers 1054 indicate support for a processor that supports both a segmented and non-segmented address space.

We submit that neither the above sections nor any other disclosure of McGrath either teach or suggest the assigning of target architecture predicate registers which may be used by the translated application to identify a target architecture register containing a base address of a segment associated with a logical address of a translated instruction, as in Claim 1.

For each of the above reasons therefore, Claim 1 and all claims that depend on Claim 1 are patentable over the cited art. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 1-10.

Each of Applicants' other independent claims includes limitations similar to those in Claim 1 discussed above. Therefore, all of Applicant's other independent claims, and all claims which depend on them, are also patentable over the cited art, for similar reasons. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(e) rejection of Claims 11-30.

Dependent Claims

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicant's silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Request for Examiner's Interview

Applicant believes that the above listed claims are in condition for allowance, and further believes that a telephone conference to discuss the allowance of these claims would greatly facilitate the examination of the subject Application. The Examiner, therefore, is respectfully requested to contact the undersigned attorney by telephone at the telephone number listed below to coordinate an Examiner's Interview.

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CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-30, patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

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Dated: February 8, 2007

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CERTIFICATE OF FASCIMILLE TRANSMISSION:
I hereby certify that this correspondence is being transmitted via facsimile to (571) 273-8300 on the date below addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Annie McNally — 02/08/2007 Date